REMARKS

Claims 1-23 are currently active.

Claims 17-23 have been added.

The Examiner has rejected Claims 1-4, 8-11 and 16 as being anticipated by Koehler. Applicant respectfully traverses this rejection.

Referring to Koehler, there is disclosed an apparatus and method for synchronization of multiple data paths and recovery from lost synchronization. Koehler teaches that 32-bit data packets are transferred to splitting circuitry 16 which splits each of the data packets into two 16-bit portions which are transferred along to respective parallel paths or pipes on 16-bit buses 18 and 20 for further processing. The splitting circuitry 16 also generates for each 16-bit portion of the data packet a synchronization code, also referred to as a sync code. As the splitting circuitry splits each data packet into two portions, which are referred to as a high portion and a low portion, it assigns to and couples with each portion a two-bit synchronous code. See column 5, lines 9-26.

Koehler teaches that after the data packets are split by the splitting circuitry, they can be processed by the circuitry that required the packet to be split. Such a circuitry is identified generically in figure 1 as reference numeral 26 and 28. The circuitry 26, 28 can be packet switching circuits that cannot be implemented in 32-bit configurations because of pin count limitations. Thus, Koehler teaches that splitting in regard to the system taught by Koehler, means shortening the size of a the data being sent. See column 5, lines 28-34. This is not striping at all in regard to Claim 3 and Claim 8. Furthermore, Koehler fails to teach or suggest the use of fabrics of a switch. The circuitry 26, 28 are switches, not fabrics of a switch.

After processing by the circuits 26 and 28, the packet portions are transferred along individual paths to the grouping circuitry 38. The grouping circuitry groups the incoming smaller packet portions back into the originally sized 32-bit packets. See column 5, lines 44-50. Koehler teaches that figure 2 shows the splitting circuitry 16. The 32-bit data packets are received and split into 2 16-bit data streams 42, 44 by a data splitter 46. The 16-bit data packet portions are afforded along the data streams 42, 44 to a high side data reformatter 52 and a low side data reformatter 54, respectively. The 18-bit data packages, which include the two-bit pcode bits are forwarded out of the splitting circuitry 16 toward the functional circuits 26 and 28. See column 5, line 53-column 6, line 2.

As is evident from the teachings of Koehler and the figures of Koehler, the functional circuits 26, 28 only receive full data from one splitting circuitry 16. There is no teaching or suggestion of each fabric receiving portions of packets from each port card as is found in applicant's invention of Claim 1.

Claims 2-4 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

Claim 8 is patentable for the reasons Claims 1 and 3 are patentable.

Claim 16 is patentable because Koehler fails to teach or suggest how to determine which one of the fabrics has the failure, as found in Claim 16.

The Examiner has indicated that Claims 5-7 and 12-15 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. The newly added Claims 17 and 20 are Claims 5 and 12, respectively, written in this way, with Claims 18 and 19, and 21-23 being Claims 6, 7 and 13-15, respectively.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-23, now in this application be allowed.

Respectfully submitted,

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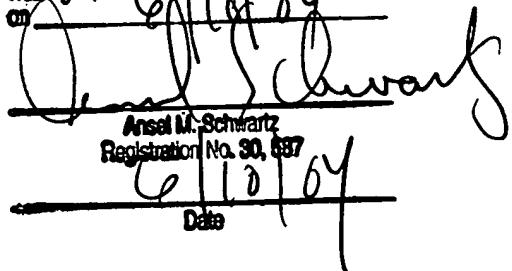Ansel M. Schwartz, Esquire
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